AMENDMENTS TO THE SPECIFICATION

At page 1 please replace the Title with the following amended Title:

COMPUTER SYSTEM EMBEDDING SEQUENTIAL BUFFERS THEREIN FOR ~~IMPROVING THE PERFORMANCE OF~~ PERFORMING A DIGITAL SIGNAL PROCESSING DATA ACCESS OPERATION AND A METHOD THEREOF

At page 13 (Abstract of the Disclosure) please replace the paragraph commencing at line 7 with the following amended paragraph:

~~Provided is a~~ A computer system embedding buffers therein for ~~improving the performance of~~ performing a digital signal processing (DSP) data access operation ~~and a method thereof. The computer system comprises~~ includes a DSP core, a data cache, first and second buffer modules, ~~and~~ an external memory and ~~. The computer system further comprises~~ a central processing unit (CPU) core. The CPU core executes instructions ~~to control operations in the system~~ and the DSP core processes data in accordance with the instructions ~~provided from the CPU core~~. The data cache stores temporary data ~~generated during operations in~~ associated with the DSP core. The first buffer module stores input data ~~forwarded to~~ received by the DSP core while the second buffer module stores output data provided from the DSP core. The external memory stores the temporary data, the input data, and the output data, wherein the input and output data are received by and provided from the DSP core in series through the first and second buffer modules without going through the data cache. ~~The computer system accesses input and output data of the DSP core by way of the first and second buffer modules and uses separated storage fields for the input data, the temporary data, and the output data, in the~~

~~external memory, which prevent degradation of the performance of the data cache and DSP functions.~~